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PATENT APPLICATION

ATTORNEY DOCKET NO. 200209576-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Mei

Confirmation No.: 8740

Application No.: 10/769,127

Examiner: Tran, Thanh Y

Filing Date: January 30, 2004

Group Art Unit: 2822

Title: FORMING A SEMICONDUCTOR

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on May 22, 2007.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Date of facsimile: June 29, 2007

Typed Name: Wendell K. Jones

Signature:

Respectfully submitted,

Mei

By

Wendell J. Jones

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07/02/2007 TL0111 00000064 082025 10769127

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Mei	Examiner:	Tran, Thanh Y.
Serial No.:	10/769,127	Group Art Unit:	2822
Filed:	January 30, 2004	Docket No.:	200209576-1
Title:	FORMING A SEMICONDUCTOR DEVICE		

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on May 22, 2007, appealing the final rejection of claims 1-10, 13-20, 22 and 23 of the above-identified application as set forth in the Final Office Action mailed January 26, 2007.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. §41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-10, 13-20, 22 and 23.

Appeal Brief to the Board of Patent Appeals and Interferences
Appellant: Mei
Serial No.: 10/769,127
Filed: January 30, 2004
Docket No.: 200209576-1
Title: FORMING A SEMICONDUCTOR DEVICE

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REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed January 26, 2007, claims 1-10, 13-20, 22 and 23 were finally rejected. Claims 11, 12, 21 and 24-30 were previously withdrawn. Claims 1-10, 13-20, 22 and 23 are pending in the application, and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed January 26, 2007. A Response After Final was filed on March 28, 2007 but no amendments to the claims were proposed by Appellants or entered by the Examiner.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The Summary is set forth as an exemplary embodiment as the language corresponding to independent claims 1 and 13. Discussions about elements of

claims 1 and 13 can be found at least at the cited locations in the specification and drawings.

The present invention, as claimed in independent claim 1, provides a method for forming a semiconductor device comprising forming a 3-dimensional (3D) pattern in a substrate and depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device. (See, e.g., specification at page 5, lines 20-25; Figure 1; reference numbers 110 and 120).

The present invention, as claimed in independent claim 13, provides a system for forming a semiconductor device comprising means for forming a 3-dimensional (3D) pattern in a substrate and means for depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device. (See, e.g., specification at page 6, lines 19 – page 7 line 5; Figures 3 and 4; reference numbers 310, 320, 330, 340, 405, 410 and 415).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

i. **Claims 1-10, 13-20 and 22-23 stand rejected under 35 U.S.C. §102(e) as being anticipated by Taussig et al (USPN 6,861,365).**

ARGUMENT

I. The Applicable Law

We respectfully remind the Examiner that in order to anticipate a claim, US Patent 6,861m365 to Taussig et al. (hereinafter *Taussig*) must teach every element of the claim and "***the identical invention must be shown in as complete detail as contained in the ... claim.***" *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989) (emphasis added).

II. Rejection of Claims 1-10, 13-20 and 22-23 under 35 U.S.C. §102(e) as being anticipated by Taussig et al (USPN 6,861,365).

The Examiner rejected Claims 1-10, 13-20 and 22-23 under 35 U.S.C. §102(e) as being anticipated by Taussig et al (USPN 6,861,365). Appellants respectfully submit that *Taussig* does not teach or suggest the invention of independent claims 1 and 13, and the claims depending therefrom.

Appellant respectfully disagrees. The present invention includes a method and system for forming a semiconductor device. Varying embodiments allow 2-dimensional alignment features to be created in 3-dimensional structures on a device substrate prior to any processing steps. Subsequent processing steps, including material deposition, planarization and anisotropic etching are utilized to construct a multi-level aligned pattern. Accordingly, the use of the method and system can potentially increase the flexibility of the semiconductor manufacturing process.

Claim 1 recites a method for forming a semiconductor device that includes forming a 3-dimensional (3D) pattern ***in a substrate*** and depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states that the Taussig reference anticipates the present invention. Appellant respectfully disagrees and asserts that ***the Taussig reference does not disclose forming a 3-dimensional (3D) pattern in a substrate as recited in claim 1 of the present invention.*** (Emphasis added.) Taussig discloses a method and system for forming a semiconductor device. The method and system involves the utilization of a stamping tool to generate 3-*D resist structures* whereby thin film patterning steps can be transferred *to the resist* in a single molding step and subsequently revealed in later processing steps.

Appellant argued in the response filed on October 23, 2006, that the Taussig reference does not disclose the formation of 3D patterns ***in a substrate*** as recited in claims 1 and 13 of the present invention. In response to this argument, the Examiner asserts that the Taussig reference clearly discloses in Figure 1 the step of forming a 3-D pattern (see step 130) in a substrate (see step 110) (also see col. 3, lines 14-30). Appellant respectfully disagrees. Col. 3, lines 14-30 read as follows:

> For a better understanding of the present invention please refer to FIG. 1. FIG. 1 is a high-level flow chart of the method in accordance with the present invention. First, a substrate is provided, via step 110. Preferably, the substrate comprises a flexible substrate adequate for use in a roll-to-roll fabrication process. Next, a layer of material is deposited over the substrate, via step 120. The material preferably comprises an organic or inorganic material. Finally, ***a 3-dimensional (3D) resist structure is formed over the first layer of material wherein the 3D resist structure comprises a plurality of different vertical heights throughout the structure, via step 130.*** Preferably, the 3D resist structure is generated by utilizing a stamping tool. Since the 3D resist structure comprises a plurality of different vertical heights throughout the structure, the structure can be utilized to transfer alignment patterns to an underlying layer based on subsequent etching steps. (Emphasis added.)

Appellant asserts that the Examiner is incorrectly correlating step 130 of the Taussig reference with the present invention of independent claims 1 and 13. Step 130 of Taussig discloses " a 3-dimensional (3D) resist structure is formed *over* the first layer of material wherein the 3D resist structure comprises a plurality of different vertical heights throughout the structure". (Emphasis added.) Appellant asserts that the first layer of material described in step 130 is the layer of material that was deposited *over* the substrate in step120. Consequently, the 3D pattern is

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formed in the layer of material that was deposited *over* the substrate and not the substrate as recited in independent claims 1 and 13.

Appellant therefore asserts that Taussig discloses the formation of a 3-D pattern in a layer of resist material *over* a substrate and therefore clearly teaches away from the formation of a 3-D pattern *in a* substrate as recited in independent claims 1 and 13 of the present invention. Appellant accordingly asserts that the Taussig reference does not disclose every element of independent claims 1 and 13. Independent claims 1 and 13 are therefore patentably distinct in view of the Taussig reference and the rejections of claims 1 and 13 under 35 U.S.C. §102(e) ought to now be withdrawn.

Claims 2-10, 14-20 and 22-23

Since claims 2-10, 14-20 and 22-23 are respectively dependent on claims 1 and 13, the above-articulated arguments with regard to independent claims 1 and 13 apply with equal force to claims 2-10, 14-20 and 22-23. Accordingly, claims 2-10, 14-20 and 22-23 should be allowed over the Examiner's cited reference.

CONCLUSION

For the above reasons, Appellants respectfully submit that the cited references neither anticipate nor render obvious claims of the pending Application. The pending claims distinguish over the cited references, and therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-10, 13-20, 22 and 23 be allowed.

Any inquiry regarding this Response should be directed to Wendell J. Jones at Telephone No. (408) 938-0980. In addition, all correspondence should continue to be directed to the following address:

IP Administration
Legal Department, M/S 35
HEWLETT-PACKARD COMPANY
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,

Mei

By their attorney,

Wendell J. Jones

Date: 6/29/07

Wendell J. Jones
Reg. No. 45,961

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CLAIMS APPENDIX

1. (Original) A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate; and

depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

2. (Original) The method of claim 1 wherein forming the 3D pattern further comprises:

depositing a layer of material onto the substrate; imprinting a 3D pattern into the layer of material; and

transferring the 3D pattern into the substrate.

3. (Original) The method of claim 1 wherein the semiconductor device comprises a cross-point memory array.

4. (Original) The method of claim 2 wherein the semiconductor device is at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

5. (Original) The method of claim 2 wherein imprinting a 3D pattern into the layer of material further comprises utilizing a 3D stamping tool to create the 3D pattern.

6. (Original) The method of claim 2 wherein imprinting a 3D pattern into the layer of material further comprises utilizing a molding process to imprint the 3D pattern into the layer of material.

7. (Original) The method of claim 2 wherein the layer of material comprises a polymer material.

8. (Original) The method of claim 2 wherein the layer of material comprises a photo-resist material.

9. (Original) The method of claim 2 wherein transferring the 3D pattern into the substrate includes:

removing a portion of the layer of material thereby exposing a portion of the substrate;

etching the exposed portion of the substrate;

removing another portion of the layer of material thereby exposing a second portion of the substrate;

etching the second portion of the substrate; and

removing a remaining portion of the layer of material.

10. (Original) The method of claim 3 wherein depositing at least one material over the substrate further comprises:

depositing two sets of conductors with a semiconductor layer there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.

11. (Withdrawn) The method of claim 9 wherein depositing at least one material over the substrate further comprises:

depositing a first metal layer on the substrate;

applying a first planarizing polymer to the metal layer;

removing a portion of the first planarizing polymer;

utilizing the first planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

etching the substrate in a selective fashion; and

removing the first planarizing polymer.

12. (Withdrawn) The method of claim 11 wherein depositing at least one material over the substrate further comprises:

depositing a second metal layer on the remaining portion of the first metal layer;

applying a second planarizing polymer to the second metal layer;

removing a portion of the second planarizing polymer;

utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

removing the second planarizing polymer.

13. (Original) A system for forming a semiconductor device comprising:

means for forming a pattern in a substrate wherein the pattern is 3-dimensional; and

means for depositing at least one semiconductor material over the substrate in accordance with desired characteristics of the semiconductor device.

14. (Original) The system of claim 13 wherein the semiconductor device comprises a cross-point memory array.

15. (Original) The system of claim 13 wherein the means for forming the pattern further comprises:

means for depositing a layer of material onto the substrate;

means for imprinting a 3D pattern onto the layer of material; and

means for transferring the 3D pattern into the substrate.

16. (Original) The system of claim 14 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing two sets of conductors with a semiconductor layer there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.

17. (Original) The system of claim 14 wherein the semiconductor device is at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

18. (Original) The system of claim 15 wherein the means for imprinting a 3D pattern into the layer of material further comprises means for implementing a molding process to imprint the 3D pattern into the layer of material.

19. (Original) The system of claim 15 wherein the means for transferring the 3D pattern into the substrate includes:

means for removing a portion of the layer of material thereby exposing a portion of the substrate;

means for etching the exposed portion of the substrate;

means for removing another portion of the layer of material thereby exposing a second portion of the substrate;

means for etching the second portion of the substrate; and

means for removing a remaining portion of the layer of material.

20. (Original) The system of claim 15 wherein the means for imprinting a 3D pattern onto the layer of material further comprises means for utilizing a 3D stamping tool to create the 3D pattern.

21. (Withdrawn) The system of claim 15 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing a first metal layer;

means for applying a planarizing polymer to the first metal layer;

means for removing a portion of the planarizing polymer;

means for utilizing the planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

means for etching the substrate in a selective fashion; and

means for removing the planarizing polymer.

22. (Original) The system of claim 15 wherein the layer of material comprises a polymer material.

23. (Original) The system of claim 15 wherein the layer of material comprises a photo-resist material.

24. (Withdrawn) The system of claim 21 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing a second metal layer on the remaining portion of the first metal layer;

means for applying a second planarizing polymer to the second metal layer;

means for removing a portion of the second planarizing polymer;

means for utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

means for removing the second planarizing polymer.

25. (Withdrawn) A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate;

depositing a first metal layer on the substrate;

applying a first planarizing polymer to the metal layer;

removing a portion of the first planarizing polymer;

utilizing the first planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

etching the substrate in a selective fashion; and removing the first planarizing polymer.

26. (Withdrawn) The method of claim 25 wherein the semiconductor device comprises a cross-point memory array.

27. (Withdrawn) The method of claim 25 further comprising:

depositing a second metal layer on the remaining portion of the first metal layer;

applying a second planarizing polymer to the second metal layer;

removing a portion of the second planarizing polymer;

utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

removing the second planarizing polymer.

28. (Withdrawn) A semiconductor device comprising:

a substrate wherein the substrate comprises a 3D pattern formed therein;

at least one material deposited thereon in accordance with desired characteristics of the semiconductor device.

29. (Withdrawn) The semiconductor device of claim 28 wherein the 3D pattern is formed with the following process:

depositing a layer of material onto the substrate;

imprinting a 3D pattern into the layer of material; and

transferring the 3D pattern into the substrate.

30. (Withdrawn) The semiconductor device of claim 29 wherein transferring the 3D pattern into the substrate includes:

removing a portion of the layer of material thereby exposing a portion of the substrate;

etching the exposed portion of the substrate;

removing another portion of the layer of material thereby exposing a second portion of the substrate;

etching the second portion of the substrate; and

removing a remaining portion of the layer of material.

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Appellant: Mei
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EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.